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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/067,038	02/04/2002	Tse-Yu Yeh	5580-04402	4972

34399 7590 05/19/2006

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/067,038	YEH, TSE-YU	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,10-12,14,15,18,23-25 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,10-12,14,15,18,23-25 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 4-5, 10-12, 14-15, 18, 23-25, and 27 have been considered. Claim 17 has been cancelled as per Applicant's request. Claims 1, 4-5, 10, 14, 18, 23, and 27 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 21 February 2006.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-5, 14-15, 18, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riordan et al., U.S. Patent Number 5,027,270 (herein referred to as Riordan) in view of Patel et al., U.S. Patent Number 5,353,426 (herein referred to as Patel).

5. Referring to claims 1 and 27, taking claim 1 as exemplary, Riordan has taught a processor comprising:

a. A control circuit, wherein the control circuit is configured to detect a replay of an instruction in a load/store pipeline due to a load miss (Riordan column 1, lines 29-33; column 2, lines 3-16; column 3, line 64 to column 4, line 8; column 4, lines 47-55; and Figure 1), and

b. Wherein the control circuit is configured to enter into a stall state and inhibit issuance of instructions to the load/store pipeline until fill data in response to the load miss is returned for loading (Riordan column 3, lines 11-38).

6. Riordan has not explicitly taught

a. A queue configured to store one or more entries identifying a cache miss, the one or more entries including a destination register field to identify a destination register associated with the cash miss and a tag associated with each destination register field to identify a fill corresponding to a cache miss for an entry; and

b. A control circuit coupled to the queue,

c. The control circuit to couple a destination register value to the queue associated with the load miss in which the queue is to respond with a fill tag associated with the destination registers the control circuit to store the fill tag in a miss tag register and to compare the fill tag in the miss tag register with fill tag of fill data being returned,

d. Wherein when a returned fill tag matches the fill tag in the miss tag register. the load/store pipeline exits the stall state.

7. However, Riordan has taught that the address of the instruction/data causing the cache miss is determined and saved (Riordan column 1, lines 29-33; column 2, lines 3-16; column 3, line 64 to column 4, line 8; column 4, lines 47-55; and Figure 1). Patel has taught

a. A queue configured to store one or more entries identifying a cache miss, the one or more entries including a destination register field to identify a destination register associated with the cash miss and a tag associated with each destination

register field to identify a fill corresponding to a cache miss for an entry (Patel Abstract; column 3, lines 18-47; column 5, line 61 to column 6, line 5; column 6, lines 15-44; column 7, lines 46-66; column 8, line 12 to column 10, line 5; Figure 3; Figure 4; and Figure 5); and

b. A control circuit coupled to the queue (Patel Abstract; column 3, lines 18-47; column 5, line 61 to column 6, line 5; column 6, lines 15-44; column 7, lines 46-66; column 8, line 12 to column 10, line 5; Figure 3; Figure 4; and Figure 5),

c. The control circuit to couple a destination register value to the queue associated with the load miss in which the queue is to respond with a fill tag associated with the destination registers the control circuit to store the fill tag in a miss tag register and to compare the fill tag in the miss tag register with fill tag of fill data being returned (Patel Abstract; column 3, lines 18-47; column 5, line 61 to column 6, line 5; column 6, lines 15-44; column 7, lines 46-66; column 8, line 12 to column 10, line 5; Figure 3; Figure 4; and Figure 5),

d. Wherein when a returned fill tag matches the fill tag in the miss tag register. the load/store pipeline exits the stall state (Patel Abstract; column 3, lines 18-47; column 5, line 61 to column 6, line 5; column 6, lines 15-44; column 7, lines 46-66; column 8, line 12 to column 10, line 5; Figure 3; Figure 4; and Figure 5).

8. A person of ordinary skill in the art at the time the invention was made, and as taught by Patel, would have recognized that the cache tag and comparator unit of Patel reduces idle time due to cache misses (Patel column 2, lines 52-63), thereby improving processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art the time the

invention was made incorporate the cache tag and comparator unit of Patel in the device of Riordan to improve processor speed and efficiency.

9. Claim 27 is substantially the same as claim 1 and is rejected for similar reasons. The only difference being claim 27 is a "computer accessible medium comprising one or more data structures to manufacture a processor" while claim 1 is a processor.

10. Referring to claim 2, Riordan in view of Patel has taught wherein the control circuit is configured to inhibit issuance of the instructions until fill data is provided to a data cache of the processor (Riordan column 3, lines 11-38).

11. Referring to claim 4, Riordan in view of Patel has taught wherein the control circuit further includes a comparator coupled to the ' miss tag register to compare the fill tag in the miss tag register to-the fill tags of returned fill data to determine if the fill data being returned corresponds to the load miss (Patel Abstract; column 3, lines 18-47; column 5, line 61 to column 6, line 5; column 6, lines 15-44; column 7, lines 46-66; column 8, line 12 to column 10, line 5; Figure 3; Figure 4; and Figure 5).

12. Referring to claim 5, Riordan in view of Patel has taught wherein multiple-lead cache misses may be present in which comparison of the miss tag register and fill tags identifies fill data to its corresponding load miss (Patel Abstract; column 3, lines 18-47; column 5, line 61 to column 6, line 5; column 6, lines 15-44; column 7, lines 46-66; column 8, line 12 to column 10, line 5; Figure 3; Figure 4; and Figure 5).

13. Referring to claim 14, Riordan has taught a method comprising:

a. Detecting a replay of a first instruction due to a dependency on a load miss in a load/store pipeline of a processor (Riordan column 1, lines 29-33; column 2, lines

3-16; column 3, line 64 to column 4, line 8; column 4, lines 47-55; and Figure 1); and

b. Inhibiting issuance of one or more instructions from a queue to the load/store pipeline responsive to detecting the replay by entering a stall state (Riordan column 3, lines 11-38).

14. Riordan has not taught

a. Sending a destination register value to a queue that stores an entry identifying the load miss, the entry including a destination register field to identify a destination register associated with the load miss and a tag associated with the destination register field of the load miss to identify a fill tag corresponding to the load miss;

b. Returning the fill tag from the queue as a miss tag:

c. Storing the miss tag corresponding to the load miss in a register;

d. Comparing the fill tag of fill data being returned to the miss tag to identify when fill data corresponding to the load miss is being returned; and

e. Exiting the stall state to allow one or more instructions to issue to the pipelines when a fill tag of fill data matches the miss tag.

15. However, Riordan has taught that the address of the instruction/data causing the cache miss is determined and saved (Riordan column 1, lines 29-33; column 2, lines 3-16; column 3, line 64 to column 4, line 8; column 4, lines 47-55; and Figure 1). Patel has taught

a. Comparing the fill tag to the tag to identify when fill data corresponding to the load miss is being returned (Patel Abstract; column 3, lines 18-47; column 5, line

61 to column 6, line 5; column 6, lines 15-44; column 7, lines 46-66; column 8, line 12 to column 10, line 5; Figure 3; Figure 4; and Figure 5);

b. Sending a destination register value to a queue that stores an entry identifying the load miss, the entry including a destination register field to identify a destination register associated with the load miss and a tag associated with the destination register field of the load miss to identify a fill tag corresponding to the load miss (Patel Abstract; column 3, lines 18-47; column 5, line 61 to column 6, line 5; column 6, lines 15-44; column 7, lines 46-66; column 8, line 12 to column 10, line 5; Figure 3; Figure 4; and Figure 5);

c. Returning the fill tag from the queue as a miss tag (Patel Abstract; column 3, lines 18-47; column 5, line 61 to column 6, line 5; column 6, lines 15-44; column 7, lines 46-66; column 8, line 12 to column 10, line 5; Figure 3; Figure 4; and Figure 5):

d. Storing the miss tag corresponding to the load miss in a register (Patel Abstract; column 3, lines 18-47; column 5, line 61 to column 6, line 5; column 6, lines 15-44; column 7, lines 46-66; column 8, line 12 to column 10, line 5; Figure 3; Figure 4; and Figure 5);

e. Comparing the fill tag of fill data being returned to the miss tag to identify when fill data corresponding to the load miss is being returned (Patel Abstract; column 3, lines 18-47; column 5, line 61 to column 6, line 5; column 6, lines 15-44; column 7, lines 46-66; column 8, line 12 to column 10, line 5; Figure 3; Figure 4; and Figure 5); and

f. Exiting the stall state to allow one or more instructions to issue to the pipelines when a fill tag of fill data matches the miss tag (Patel Abstract; column 3, lines 18-47; column 5, line 61 to column 6, line 5; column 6, lines 15-44; column 7, lines 46-66; column 8, line 12 to column 10, line 5; Figure 3; Figure 4; and Figure 5).

16. A person of ordinary skill in the art at the time the invention was made, and as taught by Patel, would have recognized that the cache tag and comparator unit of Patel reduces idle time due to cache misses (Patel column 2, lines 52-63), thereby improving processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art the time the invention was made incorporate the cache tag and comparator unit of Patel in the device of Riordan to improve processor speed and efficiency.

17. Referring to claim 15, Riordan in view of Patel has taught wherein exiting the stall state to allow one or more instructions to issue occurs after fill data is provided to a data cache (Riordan column 3, lines 11-38).

18. Referring to claim 18, Riordan in view of Patel has taught wherein multiple load misses may be present in which comparing the miss tag and fill tags identifies fill data to its corresponding load miss (Patel Abstract; column 3, lines 18-47; column 5, line 61 to column 6, line 5; column 6, lines 15-44; column 7, lines 46-66; column 8, line 12 to column 10, line 5; Figure 3; Figure 4; and Figure 5).

19. Claims 10-12 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riordan et al., U.S. Patent Number 5,027,270 (herein referred to as Riordan) in view of Patel et al., U.S. Patent Number 5,353,426 (herein referred to as Patel) and further in view of Merchant et

al., U.S. Patent Number 6,665,792 (herein referred to as Merchant). Riordan in view of Patel has not taught

a. Wherein the control circuit is configured to permit issuance of one of the one or more instructions if one or more instructions lack dependency to the load miss (Applicant's claim 10).

b. Wherein dependencies to the load miss are maintained by one or more scoreboards coupled to the control circuit (Applicant's claim 11).

c. Wherein the control circuit is configured to detect dependencies on the load miss using one or more scoreboards which track instructions that have passed a first stage of a pipeline where replay is signaled (Applicant's claim 12).

d. Permitting issuance of one of the one or more instructions if one or more instructions lack the dependency to the load miss (Applicant's claim 23).

e. Detecting lack of dependency for an instruction in one or more scoreboards (Applicant's claim 24).

f. Detecting lack of dependency for an instruction by checking one or more scoreboards which track instructions that have passed a stage of the pipeline where replay is signaled (Applicant's claim 24).

20. Merchant has taught

a. Wherein the control circuit is configured to permit issuance of one of the one or more instructions if one or more instructions lack dependency to the load miss (Applicant's claim 10) (Merchant column 1, lines 26-50; column 2, line 61 to column 3, line 7; and column 7, lines 37-51).

b. Wherein dependencies to the load miss are maintained by one or more scoreboards coupled to the control circuit (Applicant's claim 11) (Merchant column 1, lines 26-50; column 2, line 61 to column 3, line 7; and column 7, lines 37-51).

c. Wherein the control circuit is configured to detect dependencies on the load miss using one or more scoreboards which track instructions that have passed a first stage of a pipeline where replay is signaled (Applicant's claim 12) (Merchant column 1, lines 26-50; column 2, line 61 to column 3, line 7; and column 7, lines 37-51).

d. Permitting issuance of one of the one or more instructions if one or more instructions lack the dependency to the load miss (Applicant's claim 23) (Merchant column 1, lines 26-50; column 2, line 61 to column 3, line 7; and column 7, lines 37-51).

e. Detecting lack of dependency for an instruction in one or more scoreboards (Applicant's claim 24) (Merchant column 1, lines 26-50; column 2, line 61 to column 3, line 7; and column 7, lines 37-51).

f. Detecting lack of dependency for an instruction by checking one or more scoreboards which track instructions that have passed a stage of the pipeline where replay is signaled (Applicant's claim 24) (Merchant column 1, lines 26-50; column 2, line 61 to column 3, line 7; and column 7, lines 37-51).

21. A person of ordinary skill in the art at the time the invention was made, and as recognized by Merchant, would have recognized that out-of-order execution and replaying cache miss load

instructions reduces overall latency (Merchant column 1, lines 39-40) and prevents incorrect data from polluting the cache system and wasting bus resources (Merchant column 3, lines 1-7), thereby increasing performance (Merchant column 1, lines 39-40) and ensuring correct data is executed on. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the out-of-order execution and replay of Merchant in the device of Riordan to increase performance and ensuring correct data.

Response to Arguments

22. Applicant's arguments with respect to claims 1-2, 4-5, 10-12, 14-15, 18, 23-25, and 27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Morein, U.S. Patent Number 6,353,874; Bronstein et al., U.S. Patent Number 6,633,565; and Favor, U.S. Patent Number 6,732,236 have taught a cache miss system storing the cache miss locations and comparing tags.

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

25. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

27. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

28. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
12 May 2006

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